

**PRINTED CIRCUIT BOARD ASSEMBLY AND METHOD**

Technical Field

[0001] The present invention generally relates to printed circuit board assemblies having integrated circuits soldered thereto.

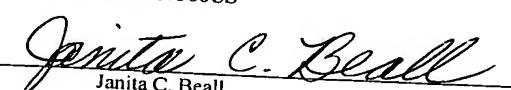
Background of the Invention

[0002] A conventional IC 10 (Fig. 1) includes a leadframe 11 with leads 12 that extend from the centerline of the package body 13. The leads 12 are formed in a gullwing shape to create solderable feet for mounting to printed circuit boards ("PCB"). "Leadless" IC packages have also been developed, two examples of which are known as Micro-LeadFrame (MLF) and Quad-Flat Pack - No-Lead (QFN). The electrical contacts for such IC packages are generally located on the bottom of the molded body, and the IC package has a much smaller footprint and weight. A QFN or MLF will generally have significantly lower total pin inductance due to the much shorter lead length. Thus, QFNs and MLFs are suitable for higher frequency applications such as the RF portion of wireless devices.

[0003] Various problems have been encountered in obtaining a reliable solder connection when a MLF or QFN is assembled to a printed circuit board. During fabrication, an array of ICs is generally fabricated utilizing a molding processes. The array is cut into individual ICs during singulation, thereby exposing unplated copper at the electrical contacts. A good solder fillet at the electrical contacts is required for reliability. Achieving a satisfactory solder fillet may be difficult because the uncoated copper oxidizes, such that commonly available solder paste does not achieve a fillet having sufficient strength for many applications. A more active flux may be utilized to alleviate the effects of the oxidation. However, use of active flux creates a high risk of dendritic growth in the solder, resulting in an unreliable joint.

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Summary of the Invention

[0004] One aspect of the present invention is a method of fabricating a printed circuit board assembly. The method includes molding an array having a plurality of integrated circuits that are physically interconnected. Each integrated circuit has a molded body defining a lower surface. The integrated circuits have a plurality of electrical contacts on the bottom surface. The method includes singulating the array to form a plurality of separate integrated circuits, and at least a portion of the electrical contacts are cut. An organic solderability preservative is applied to the cut portion of the electrical contacts. Heat is applied to the integrated circuits to dry the circuits, and the integrated circuits are soldered to a printed circuit board by applying molten solder to remove the organic solderability preservative.

[0005] Another aspect of the present invention is a method of fabricating an integrated circuit package. The method includes molding an array including a plurality of integrated circuits that are physically interconnected. Each integrated circuit has a molded body defining a lower surface, and each integrated circuit has a plurality of electrical contacts on the bottom surface. The array is singulated into a plurality of separate integrated circuits by sawing the array. An organic solderability preservative is applied to at least a portion of the electrical contacts, and heat is applied to dry the organic solderability preservative.

[0006] These and other features, advantages and objects of the present invention will be further understood and appreciated by those skilled in the art by reference to the following specification, claims and appended drawings.

Brief Description of the Drawings

[0007] The present invention will now be described, by way of example, with reference to the accompanying drawings, in which:

[0008] Fig. 1 is a partially schematic view of a prior art IC having a leadframe;

- [0009] Fig. 2 is a fragmentary, partially schematic view of a printed circuit board assembly including a "leadless" IC according to one aspect of the present invention;
- [0010] Fig. 3 is a fragmentary, cross-sectional view of the printed circuit board assembly of Fig. 2;
- [0011] Fig. 4 is a flow chart illustrating a first embodiment of a method according to one aspect of the present invention;
- [0012] Fig. 5 is a flow chart illustrating a first embodiment of a method according to another aspect of the present invention; and
- [0013] Fig. 6 is a flow chart illustrating a first embodiment of a method according to yet another aspect of the present invention.

Description of the Preferred Embodiments

- [0014] For purposes of description herein, the terms "upper," "lower," "right," "left," "rear," "front," "vertical," "horizontal," and derivatives thereof shall relate to the invention as oriented in Figs. 2 and 3. However, it is to be understood that the invention may assume various alternative orientations and step sequences, except where expressly specified to the contrary. It is also to be understood that the specific devices and processes illustrated in the attached drawings and described in the following specification are simply exemplary embodiments of the inventive concepts defined in the appended claims. Hence, specific dimensions and other physical characteristics relating to the embodiments disclosed herein are not to be considered as limiting, unless the claims expressly state otherwise.
- [0015] With reference to Figs. 2 and 3, a MLF/QFN IC 1 includes a plurality of electrical conductors 2 on the bottom 3 of a molded IC body 4. A die 5 (Fig. 3) having the electrical circuit is secured to a die paddle 6. The lower surface 7 of the die paddle 6 is exposed, and may be utilized to mount the IC 1 directly to a printed circuit board 8. A plurality of wires 15 electrically interconnect the conductive feet 2 to the die 5, and are encapsulated in the molded body 4.

[0016] During fabrication of the integrated circuit 1, an array of MLF or QFN ICs 1 are fabricated utilizing a known molding method. With reference to Fig. 4, the MFL/QFN array is then loaded into a singulation saw machine that cuts the array to form individual ICs 1. In the preferred method of Fig. 4, an organic solderability preservative (OSP) or other agent that inhibits oxidation is added to the cutting fluid of the singulation saw. The cutting fluid and OSP are applied to the ICs 1 during the singulation process. The ICs are then dried in an oven, followed by testing and packaging. The ICs 1 are then soldered to a PCB 8 (Figs. 2 and 3) having conductors 16 and electronic components 17. Significantly, the OSP prevents oxidation of the copper or other conductors 2, such that the solder 18 forms a relatively large fillet 18, thereby forming a very strong and reliable bond between the IC 1 and the circuit board 8. Although an imidazole OSP such as ENTEK PLUS is currently preferred, various materials could be utilized to coat the conductive leads 2 to prevent oxidation of the conductors 2.

[0017] As discussed above in connection with Fig. 4, the OSP material is preferably added to the cutting fluid, and the IC 1 is singulated using a saw having OSP in the cutting fluid. Alternately, as illustrated in Fig. 5, the OSP may be applied to the IC 1 immediately following the singulation process using a dip or spray application. As illustrated in Fig. 5, it is preferred to utilize a singulation saw to singulate the ICs. However, a punch machine may also be utilized to singulate the ICs 1. The OSP would then be applied to the ICs after singulation.

[0018] With further reference to Fig. 6, if oxides have formed on the ICs after singulation, the oxides may be cleared utilizing an etch material according to known processes. The etch material is then rinsed off the parts, and the OSP is applied to the IC using a dip or spray application. After application of the OSP, the ICs 1 are oven dried and assembled to a printed circuit board 8.

[0019] The use of the OSP or other agent to prevent oxidation ensures that a strong, reliable solder connection to the PCB 8 is formed. Although

OSPs have been utilized to prevent oxidation of printed circuit boards, the use of an OSP to prevent oxidation of the leads of an IC as described above is believed to be unique.

[0020] It will be understood by those who practice the invention and those skilled in the art, that various modifications and improvements may be made to the invention without departing from the spirit of the disclosed concept. The scope of protection afforded is to be determined by the claims and by the breadth of interpretation allowed by law.